



SG1010 StarFabric Switch

Hardware Implementation Guide

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Preface

This document serves as a guide for hardware designers using StarGen's SG1010 Star-Fabric switch device. Implementation requirements will vary depending on the specific application. If you need additional information, email StarGen at support@stargen.com or refer to one or more of the documents under **Associated Documents** below.

Overview

This manual contains the following chapters and a glossary,:

- Chapter 1 Introduction – Provides an overview of the SG1010.
- Chapter 2 Power Subsystem Requirements – Defines power and ground requirements.
- Chapter 3 Routing and Layout – Discusses transmitter and receiver characteristics.
- Chapter 4 Connector and Cable Implementation – Describes serial interface and pin assignments.
- Chapter 5 Termination Requirements – Describes pin terminations, reset strap options, and receiver terminations.
- Chapter 6 Serial ROM Requirements – Defines application dependency.
- Chapter 7 EMC Considerations – Provides a list of EMC design guidelines
- Chapter 8 LED Usage – Defines modes of operation.
- Chapter 9 Diagnostic Interfaces – Describes compliance issues and CSR's.

Associated Documents

For additional information, refer to one or more of the following reference documents:

PCI Industrial Computer Manufacturer's Group (PICMG) Specifications

PICMG 2.0 D3.0, CompactPCI Specification

PICMG 2.1 R1.0, CompactPCI Hot Swap Specification

PICMG 2.17 StarFabric Specification

StarGen Specifications

StarGen, Inc. SG1010 Hardware Reference Manual

StarGen, Inc. SG1010 Data Sheet

StarGen, Inc. Fabric Programmer's Manual

StarFabric Trade Association Specifications

StarFabric Architecture Specification

IEEE Standards

IEEE Std 1149.1-1990 IEEE Standard Test Access Port and Boundary-Scan Architecture w/IEEE Std. 1149.1a-1993 and IEEE Std. 1149.1b-1994 (aka 1149.1-2001)

IEEE Std 1596.3-1996 IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)

ANSI Standards

ANSI/TIA/EIA-644-95 Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits

Revision History

Revision Number	Date mm/dd/yy	Description
0.1	06/21/02	Initial Revision of Document
1.0	08/21/03	1. Added EMC section 2. Modified the Power Subsystems section

Revision Number	Date mm/dd/yy	Description
1.1	11/02/04	1. Updated Figure 2-4. The CDR power pins were incorrectly labeled 2. Fixed a typo in Section 2.3 - VDDG is power for the 112.5Mhz PLL not the 78 Mhz PLL.
1.2	11/04/04	1. Updated section 5.2. There was a typo regarding the PLL oscillator frequency. It should be 112.5 Mhz not 78 Mhz.

Introduction

StarGen's SG1010 StarFabric Switch provides low cost high speed serial switching functionality within StarFabric, a universal switch fabric. The SG1010 provides 30 Gbps of aggregate, non-blocking, full-duplex switching capacity through six links. A link is composed of a transmitter and a receiver. Each transmitter and receiver consists of four aggregated 622 Mbps LVDS pairs. This provides 2.5 Gbps bandwidth in each direction. These links can be used to connect either to other switch nodes or to edge nodes. In addition, two SG1010 links can be connected to another Starfabric node to create a 5Gbps full duplex path between the nodes. By connecting the SG1010's LVDS interfaces to other StarFabric switches or to StarFabric edge nodes such as StarGen's SG2010 PCI-to-StarFabric bridge, flexible topologies can be designed to fit specific application requirements for bandwidth, reliability, and scalability.

The SG1010 LVDS interface is compliant with the IEEE 1596.3 and TIA/EIA-644 Low-Voltage Differential Signaling standards. The SG1010 supports address-routed traffic which provides 100% P-P bridge compatibility with existing PCI software including configuration, BIOS, OS, and drivers. The SG1010 also supports enhanced StarFabric-native path- and multicast- routed traffic.

Example applications for the SG1010 include:

- Multi-Service Access Platforms
- DSLAMs-DSL Access Multiplexers
- PCI Expansion Applications
- Voice Over IP Gateways (VOIP)
- Edge Routers/Switches
- Wireless Basestations
- Computer Telephony Integration platforms

1.1 System Design

This document is intended to assist hardware design engineers incorporate the SG1010 switch into systems. Given the variety of applications and flexibility of Starfabric, it is difficult to anticipate all possible system design issues. Email support at support@star-gen.com is available to assist with specific questions not answered in this or the reference documents.

One feature of the SG1010 switch is bundled links. These are links whereby the same two nodes in a fabric are connected by two physical links. There are restrictions imposed on the links and the supported modes when using bundled links. Please see Section 5.5 for more details.

Power Subsystem Requirements

2.1 Power Subsystem Overview

In determining the layer stack in printed circuit board (PCB) design, it is important to consider the power and ground requirements first. To help control transmission line impedances it is recommended that multi-layer board structures be used with solid uniform power and ground planes. Using solid planes also improves the power distribution for the board. Routing signals over partial power planes will cause impedance discontinuities. It may be helpful to stack power and ground planes next to each other as this forms a parallel plate capacitor that aids in filtering power supply noise. Reducing the separation between these two planes increases the capacitance between them. Common ground planes should be connected with numerous vias to help ensure good current return flow.

2.2 Power and Ground Planes

The SG1010 requires +3.3V for I/O and +1.5V for core, CDR, and PLL power. Separate power/ground plane pairs are recommended for the IO and core voltages. Partial planes or wide etch are recommended for both the PLL and CDR power. Power and ground plane splits should be avoided, but if a split is used, avoid routing high-speed signals over it. Several high-frequency capacitors should be placed across plane splits to provide a return path for common mode AC current.

2.3 Voltage Regulation

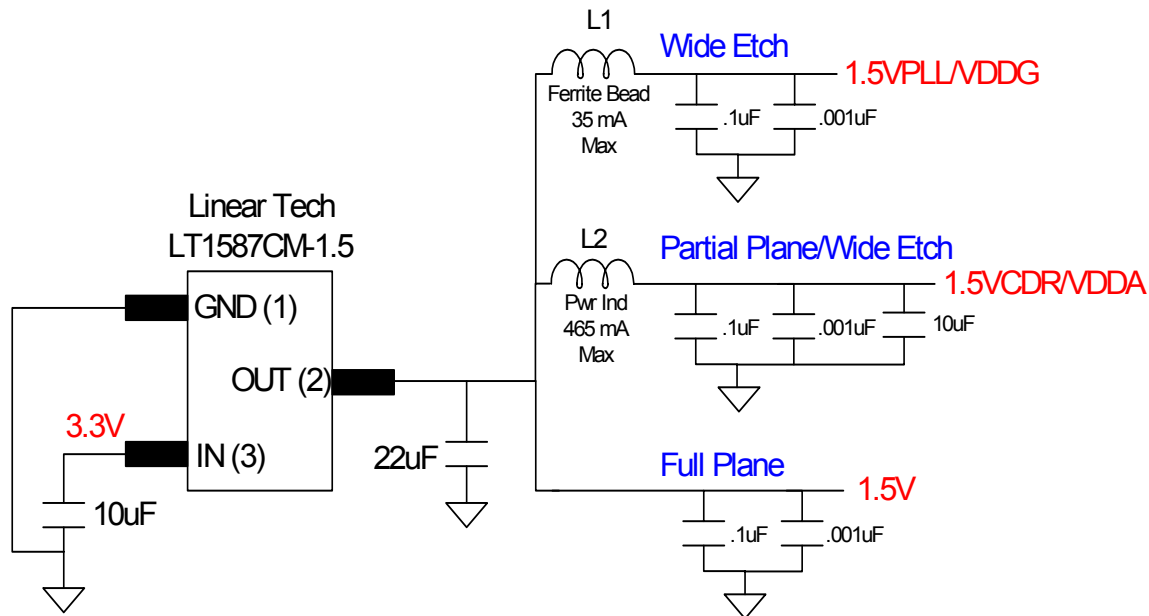
The SG1010 requires two supplies, 3.3V and 1.5V. Each should be supplied at +/- 5%. The 1.5V supply is split up into three different references V15 (power for the core), VDDG (power for the 112.5Mhz internal PLL), and VDDA (power for the Link interface). The 3.3V supply (V33) provides the power for the I/O interface of the SG1010. The maximum, worst case current requirement for each of the supplies is listed below.

- V33: 320 mA
- V15: 1100 mA

An adequate supply or voltage regulator circuit must be provided for each voltage 1.5V and 3.3V. Many system platforms provide an adequate 3.3V source. If a 1.5V supply is not available, it can be derived from the 3.3V supply with a simple regulator circuit as

shown in Figure 2–1. The full plane (1.5V) should be connected to the V15 pins and the partial planes or wide etch, 1.5VCDR and 1.5VPLL, should connect to the VDDG and VDDA pins respectively. Careful consideration should be taken when choosing the inductors required for the circuit. The inductors need to be able to handle the current required by each reference.

Figure 2–1 1.5 Voltage Regulator Circuit



Example Inductors		
Ind	Vendor	Vendor_PN
L1	Coilcraft	0603CS-R12X_BC
L2	Coilcraft	DS1608C-222

If an implementation requires a 1.5V supply for multiple devices, a switching regulation circuit may be needed to supply the necessary current. For SG1010 designs that require only a few SG1010's, Linear Technology's LT1587CM-1.5 has been successfully used. Refer to vendor data sheets for specific implementation guidelines for the selected regulator.

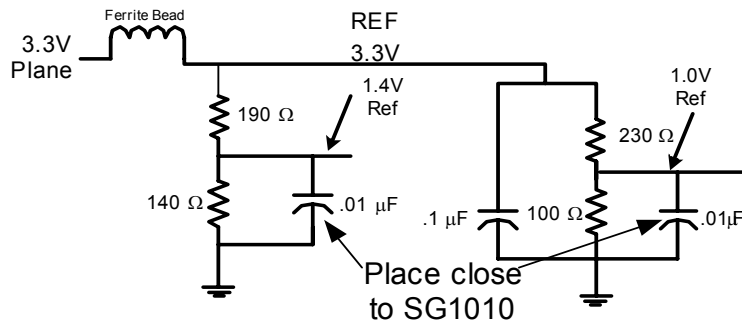
2.4 Reference Voltages

2.4.1 LVDS Transmitter Reference

In addition to the +3.3V and +1.5V supplies, the SG1010 requires reference voltages for the LVDS transmitters. These are nominally 1.0Vdc and 1.4Vdc values applied to the REF10 (BGA location C3) and REF14 (BGA location A2) input pins respectively. It is acceptable to derive these from other supplies using a resistor divider network as shown in Figure 2–2. It is important to provide stable and clean power for these references to minimize noise. A choke circuit for the divider is recommended. High-fre-

quency decoupling of 0.01 μ F should be placed as close to the SG1010 REF10 and REF14 device pins as possible, and the circuit should be connected to the reference pins with wide low impedance copper etch.

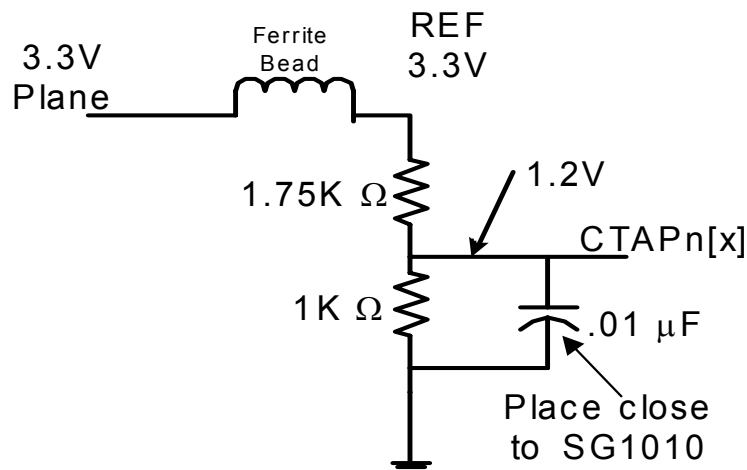
Figure 2–2 Example REF10 and REF14 circuit



2.4.2 LVDS Receiver Reference

If AC-coupling is used at the SG1010 receivers, a V_{common} Recovery circuit will be required to re-establish the DC reference for the differential signals at the SG1010. This voltage is nominally 1.2V and can also be derived with a resistor divider network (from the +3.3V or +1.5V supplies). The SG1010 has twenty-four CTAP pins (4 CTAP pins per link). To help save board real estate and reduce the part count, the four CTAP within a link can be grouped together to a circuit similar to the one shown in Figure 2–3. If SG1010 receivers are DC coupled the CTAPn[x] pin should be tied to a .01 μ F cap to ground.

Figure 2–3 V_{common} Recovery Circuit



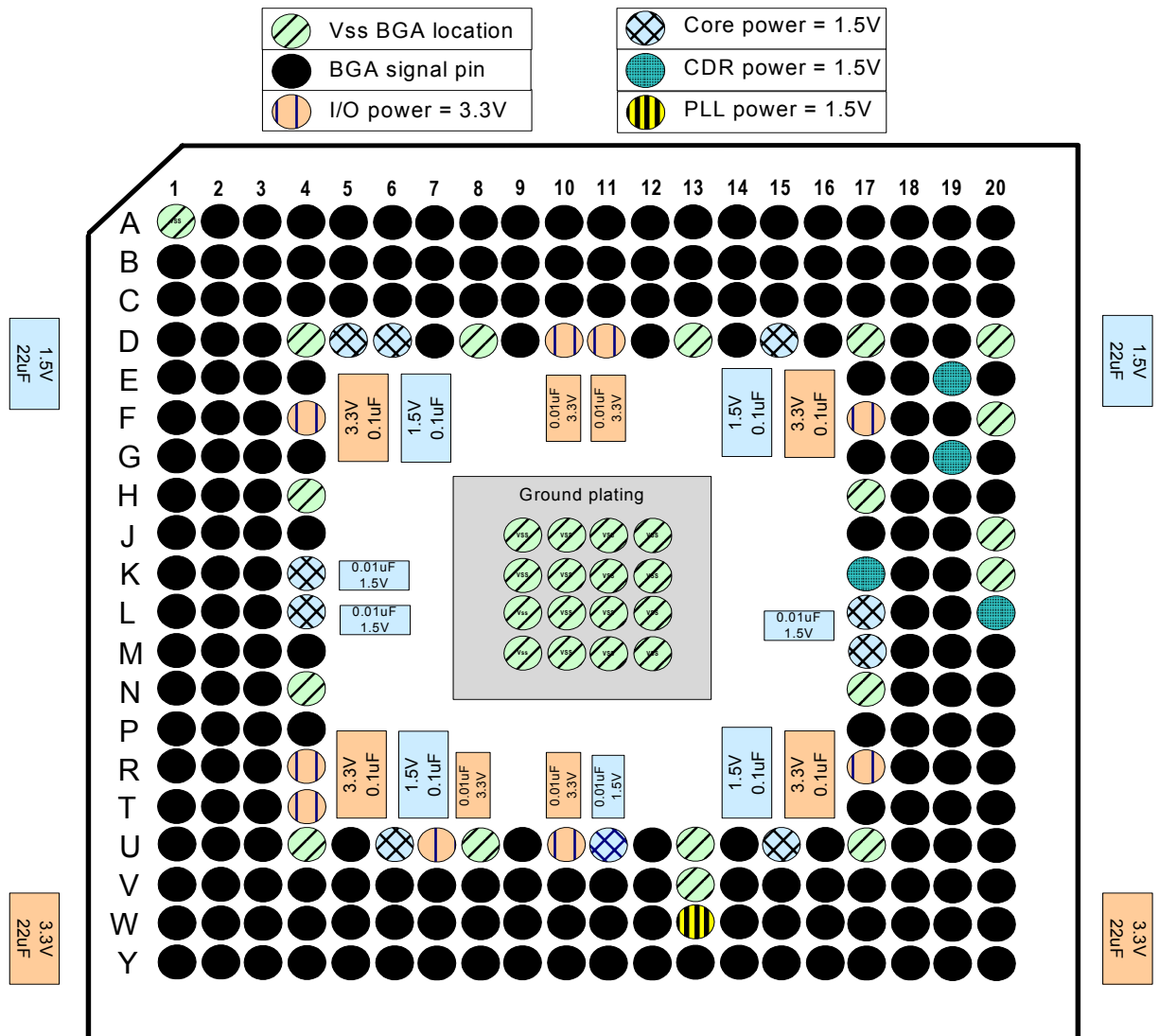
2.5 Decoupling

Good power decoupling for all active components is necessary. A combination of bulk capacitance and the use of high-frequency, low inductance local capacitance for each IC are recommended. The bulk decoupling capacitors should be distributed evenly over the board for each supply. The high-frequency capacitors should be placed as close as possible to the power pins that they are decoupling.

2.5.1 SG1010 Decoupling

Local low inductance high frequency capacitors should be placed as close as possible to the SG1010 for each power/ground pin pair. Bulk capacitors should also be used to provide stable 1.5V and 3.3V references for the SG1010. Figure 2–4 depicts a typical design with the capacitors on the opposite side of the PCB from the SG1010.

Figure 2–4 Typical Decoupling for SG1010



Routing and Layout

3.1 Routing Overview

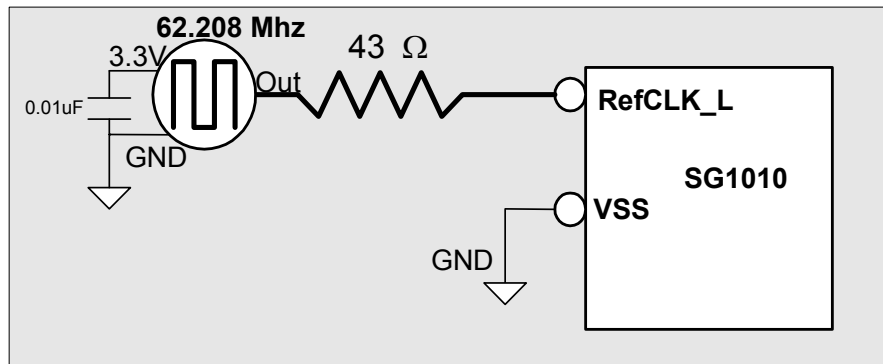
The use of signal traces with sharp 90° or greater turns should be avoided because this is a source of impedance discontinuity at high frequencies. Using chamfered turns or 45° bends are recommended alternatives. Components that terminate to a power plane, such as bypass capacitors connecting to ground, should keep their traces as short as possible for a low impedance connection.

3.2 Oscillator Requirements

The SG1010 has an on-chip phase locked loop (PLL) that is used for the clock and data recovery (CDR) of the serial transmissions. An external 62.208 MHz crystal oscillator is required for operation. This clock source should be placed close to the SG1010 IC's REFCLK_L input pin (B3) to reduce radiated noise from the components and the connecting etch. The frequency deviation should not exceed 25ppm, and the peak to peak jitter should not exceed 100ps.

A series damping resistor between the oscillator and SG1010 REFCLKL pin is recommended to create a source terminated transmission line. It is also recommended that a high frequency bypass capacitor be placed between the power and ground pins. The designer may consider using a more robust power supply filtering circuit, such as a choke circuit (not shown in example), for the oscillator. See Figure 3–1 for an example circuit.

Figure 3–1 Oscillator Routing



3.3 LVDS Routing

3.3.1 LVDS Serial Transmitter and Receiver Characteristics

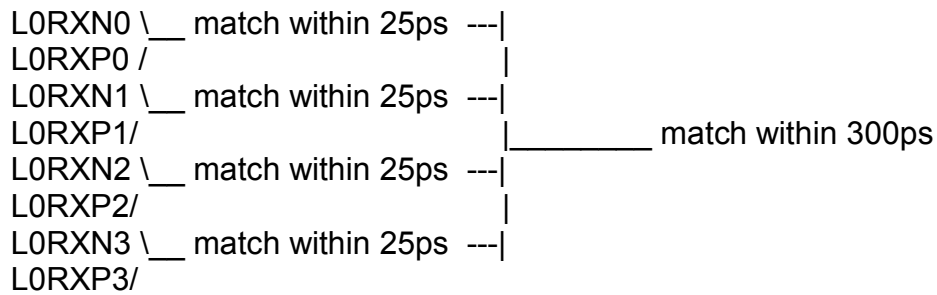
The serial transmitters and receivers used in StarGen devices are compatible with the TIA/EIA-644 and IEEE 1596.3 LVDS specifications. They transfer data at a 622Mbps rate with a loop current between 2.5mA and 4.5mA. Each transmitter has on-chip termination to minimize reflections and improve signal integrity across backplanes and connectors. Each receiver has an internal 100Ω nominal resistor that provides the required impedance to produce a voltage across the receiver. This voltage is typically 400mV with a center point at +1.2V. The receiver provides +/- 100mV sensitivity over a common-mode range of 0V to 2.4V and compensates for skew between differential pairs for proper detection. The LVDS pairs may be AC coupled. If they are, a Vcommon recovery circuit is required at the receiver end to properly restore a DC value.

3.3.2 LVDS Transmission Lines

Because of the low voltage swing and high-speed nature of LVDS, special attention must be paid to these signals. Due to the LVDS routing requirements, it is recommended that LVDS routing be completed before CMOS or TTL signals. On a circuit board, each differential signal pair should have its traces routed as close to each other as possible once they leave the IC package to produce a tightly coupled transmission line. The maximum recommended skew between the + and - signals *within* each differential pair should be no more than 25ps.

Tight control of etch length *between* pairs in a link is not necessary, but significant differences should be avoided. StarGen recommends a maximum time skew of 300ps between the four differential pairs that comprise an SG1010 link. Figure 3–2 shows the LVDS skew requirements for one SG1010 link.

Figure 3–2 LVDS Skew Requirements



The LVDS portion/layers of the circuit board must be constructed with controlled transmission line impedance of 50Ω (100Ω differential). Trace impedance should be controlled within +/- 10%, but +/- 5% control is recommended. To accomplish this, either microstrip or stripline fabrication technique can be used.

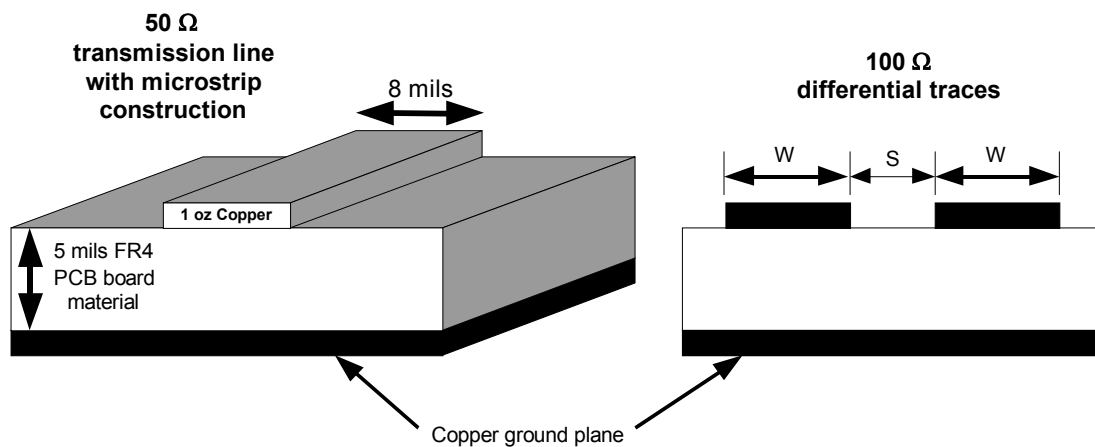
StarGen recommends the use of separate PCB layers for LVDS signals if possible. If the LVDS is routed on the same layer as digital CMOS or TTL signals, then a minimum distance of ~30 mils should be maintained between the digital signals and the LVDS signals.

3.3.3 LVDS Routing Options

3.3.3.1 Microstrip LVDS Routing

Microstrip transmission lines (Figure 3–3) are created when signal traces are routed on an outer layer of a printed circuit board over a ground plane.

Figure 3–3 Microstrip Transmission Line



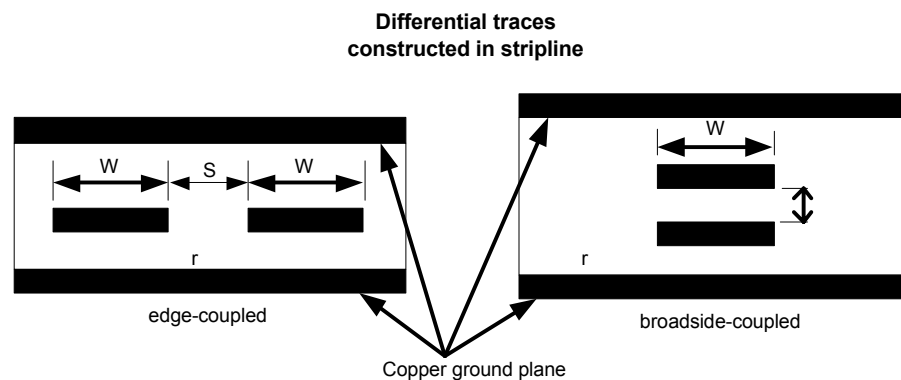
Two single-ended 50Ω transmission lines need to be constructed in PCB etch for each LVDS differential pair. Line to line spacing between the differential signals should be less than the dielectric thickness separating the traces from their reference plane (which is less than 5 mils for the microstrip example above). A line to line spacing between 1

to 3 mils is recommended. To design the 100Ω differential impedance, the width of the traces should be adjusted appropriately. An advantage of microstrip construction (Figure 3–3) is that it is possible to route traces directly from a source pin to a destination without the need of vias. Minimizing the number of vias is important for maintaining good signal quality. A disadvantage with microstrip is that it can limit the number of routing channels on a circuit board.

3.3.3.2 Stripline LVDS Routing

Stripline (Figure 3–4) is constructed by routing traces on an inner layer between two reference planes (power or ground).

Figure 3–4 Stripline Transmission Line



Traces can be edge coupled (side-by-side), or broadside coupled (one above the other). Stripline provides additional shielding that helps to reduce noise coupling onto the signal lines and aids in limiting radiation. However, inner layer signals require the use of vias and typically add layers to the circuit board. Stripline also slows down a signal's propagation velocity. Broadside constructed stripline increases the number of available routing channels at the cost of a more complex fabrication process.

For either construction technique, the distance *between* differential pairs should be a minimum of $2S$, where “ S ” is the spacing between the positive and negative sides of a differential pair. 20 mil separation or more is recommended if there is sufficient room. Also, the differential signals should be routed over a continuous uniform power plane. Vias and stubs should be minimized/avoided.

3.3.4 Summary of LVDS Routing Recommendations

The following list summarizes the LVDS routing recommendations:

- The distance *between* differential pairs should be a minimum of $2S$. 20 mil separation or more is recommended.
- The LVDS portion/layers of the circuit board must be constructed with controlled transmission line impedance of 50Ω (100Ω differential).

LVDS Routing

- Trace impedance should be controlled within +/- 10%, but +/- 5% control is recommended.
- A minimum distance of ~30 mils should be maintained between the digital signals and the LVDS signals.
- The maximum recommended skew between the + and - signals *within* each differential pair should be no more than 25ps.
- StarGen recommends a maximum time skew of 300ps between the four differential pairs that comprise an SG1010 link.
- LVDS routing should be completed before digital CMOS and TTL routing.

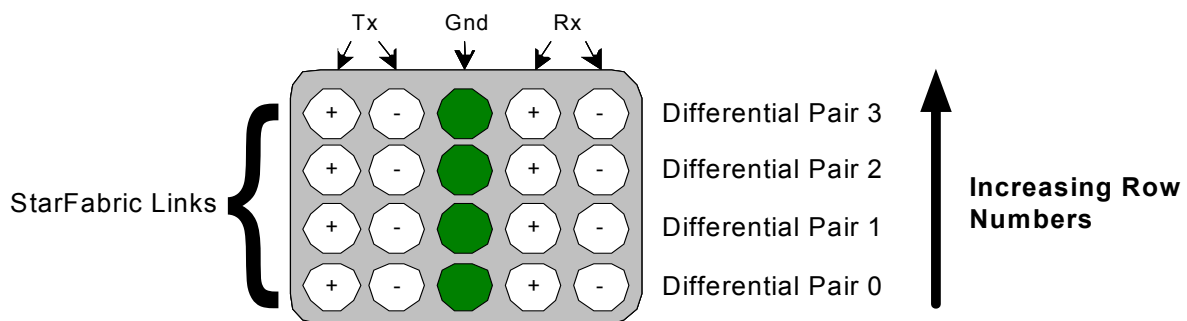
Connector and Cable Implementation

4.1 Recommended LVDS Pin Use for CompactPCI Connectors

Standard CompactPCI connector locations for the LVDS signal routing is defined by the PICMG 2.17 StarFabric Specifications. PICMG 2.17 defines two board types for use of StarFabric components. These are (1) Fabric boards that will be used for providing switch capability (with components like the SG1010 StarFabric switch) and (2) Node boards that will contain StarFabric bridge devices and could potentially contain boards with SG1010 devices or other switch devices.

For node boards, the recommended LVDS signal mapping utilizes one row of a CompactPCI connector for two differential pairs. One of these differential pairs is used for Tx+ and Tx- while the second is used for Rx+ and Rx-. With this mapping, a single full-duplex StarGen link utilizes four rows on a CompactPCI 2mm connector as shown in Figure 4-1.

Figure 4-1 Link Signal Mapping



Refer to the PICMG 2.17 StarFabric specification for more details and options.

4.2 Cable Implementation

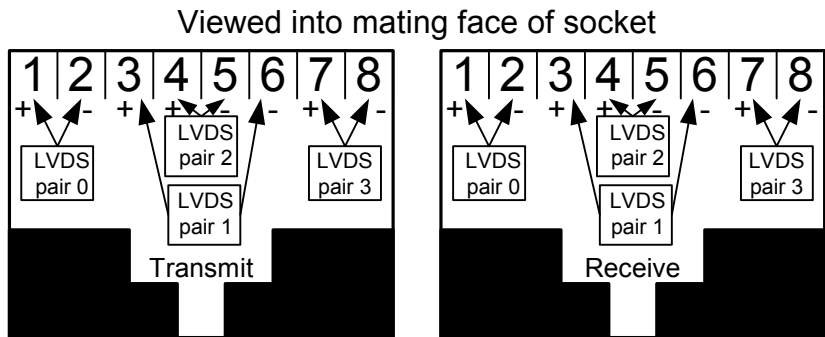
For cable applications, the LVDS serial interface on the SG1010 can be connected using a variety of interconnect choices. RJ45 connectors and cable recommendations are described below.

Cable Implementation

4.2.1 RJ45 LVDS Pin Assignments

If RJ45 connectors are used for cable interconnect, one connector should be used for the four transmit differential pairs in a link. A second RJ45 should be used for the four receive differential pairs in a link. To help save board real-estate, dual RJ45 connectors can also be used. The pin order for transmit and receive differential pairs is shown in Figure 4–2.

Figure 4–2 RJ45 Pin Order



4.2.2 CAT5 Use Guidelines

Cable interconnect can be accomplished with Category 5E cable up to **40 feet** in length. This length may be reduced, dependant upon the cable quality or type. When cable is used to connect chassis with different ground potential, AC coupling for the LVDS receivers is recommended. AC termination implementation and re-establishment of the DC Vcommon voltage on the LVDS receiving node is discussed in Section 5.4.

Termination Requirements

5.1 Pin Terminations

5.1.1 Factory Test Signal Termination

The Signals listed in Table 5–1 are not required for SG1010 applications. They are internally terminated and should be left as NO CONNECTS for all applications.

Table 5–1 Signals Always Terminated with NO CONNECT

Signal Name	BGA Location	External Termination
tstshfld	U16	No-connect
ecsel	V17	No-connect
etoggle	W18	No-connect
exdnup	Y19	No-connect
tstphase	V18	No-connect
scan_ena	U3	No-connect
testrst	W20	No-connect
tstclk	U19	No-connect
bypassl	V19	No-connect
resetx	W19	No-connect
loopbken	Y20	No-connect
scan_clk	V2	No-connect

5.1.2 JTAG and Other Pin Termination Requirements

Table 5–2 provides termination requirements for the JTAG, TESTMODE[4:0], TST-CLKG and DIAG_EN. Use of these signals are optional. If not used, they should all be terminated as shown in the table.

If the JTAG interface is not being used, it is recommended that the TRST_L signal be pulled down with a 10kΩ resistor. For designs that use more than one StarFabric device (SG2010 or SG1010), designers should be aware that each device has an internal 50 K ohm pull-up resistor and a stronger pull-down should be used on TRST_L. If the

SG1010 TRST_L signal is not pulled down, the SG1010 will operate normally but the JTAG interface is active. When the JTAG interface of the SG1010 is accessed, normal chip operation is not guaranteed.

If it is desirable to control Testmode features for an application, then TESTMODE[4:0] can be tied to a DIP switch or an option can be provided to pull one or more of these pins to 3.3V via a strapping resistor. For normal operation, they should all be pulled to GND. The TSTCLKG signal can be left as a NO CONNECT. If the capability of running the SG1010 in PLL Bypass mode is desired, it can be connected to a 112.5Mhz oscillator through a series termination resistor of $\sim 40 \Omega$. This is not necessary or recommended. DIAG_EN is used to control whether the SG1010 is set in diagnostic mode; DIAG_EN = low -> non-diagnostic mode, DIAG_EN = high -> diagnostic mode. If a diagnostic interface is not implemented this signal should be pulled to GND. For more details on the diagnostic interface please refer to Section 9.2.

Table 5–2 JTAG and Other Terminations

Signal Name	BGA Location	External Termination
trst_l	U1	10k Ω Pulldown
tck	T2	No-connect
tms	T3	No-connect
tdi	V1	No-connect
tstclk	W9	No-connect
testmode[4]	R3	10k Ω Pulldown
testmode[3]	U5	10k Ω Pulldown
testmode[2]	Y3	10k Ω Pulldown
testmode[1]	Y4	10k Ω Pulldown
testmode[0]	V5	10k Ω Pulldown
diag_en	P4	10k Ω Pulldown

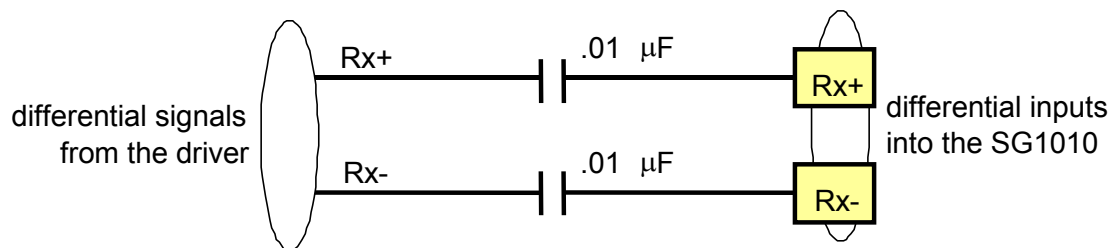
5.2 LVDS 100 Ohm Reference

The RESHI and RESLO pins on the SG1010 must be connected to each other through a 100 Ω , 1% resistor. This is used for LVDS termination reference within the SG1010.

5.3 Optional AC-Coupling for LVDS Receivers

AC-coupling at the LVDS receivers is recommended for cable applications and those where there may be a difference in ground potential between the sending and receiving SG1010 (or other StarFabric devices). To accomplish this, a $0.01\mu\text{F}$ series capacitor must be placed in series with each of the Rx+ and Rx- signal pins on the SG1010. The exact location is not important, but placement close to the connector relieves congestion around the SG1010.

Figure 5–1 AC- Coupling



5.4 LVDS Receiver Termination

The SG1010 device provides a center-tap pin for each LVDS differential pair. These twenty-four signals are labeled CTAP{5:0}[3:0]. Each pin can be individually tied to ground with a $0.01\mu\text{F}$ capacitor or a single $0.01\mu\text{F}$ capacitor can be shared for the four differential pairs in a link to save PCB real estate. If AC-termination is used at the SG1010 LVDS receivers, a V_{common} recovery voltage must also be applied to the CTAP input signals. This is nominally $+1.2\text{V}$ dc. An example circuit is shown in Figure 2–3.

5.5 Bundled Links

High bandwidth applications may require bundled links, 2 links from one StarFabric Device are connected to 2 links of another device. If a bundle is detected, the SG1010 automatically combines the 2 links, creating a 5 Gb/s link as opposed to the normal 2.5 Gb/s. There are two restrictions when using bundling:

1. The ordering of the links has to be consistent (Low link # -> Low link #)
2. If non-sequential links are used to create the bundle any links in between can not be used

5.5.1 Link Ordering

The lower link number from 1 StarFabric device has to connect to the lower link number of its link partner.

Illegal Configuration

- SG2010 Link 0 -> SG1010 Link 5

- SG2010 Link 1 -> SG1010 Link 4

Legal Configuration

- SG2010 Link 0 -> SG1010 Link 3
- SG2010 Link 1 -> SG1010 Link 4

5.5.2 Sequential Link Numbers

If contiguous links are not used, any links in between cannot be used. **(Using contiguous links is recommended).**

Illegal Configuration

- SG2010 1 Link 0 -> SG1010 Link 2
- SG2010 1 Link 1 -> SG1010 Link 4
- SG1010 Link 3 -> CANNOT connect to a StarFabric device

Legal Configuration

- SG2010 1 Link 0 -> SG1010 Link 0
- SG2010 1 Link 1 -> SG1010 Link 1
- SG1010 Link 3 -> SG2010 2 Link 0 or SG2010 2 Link 0

Table 5–3 Recommended Bundling Configurations

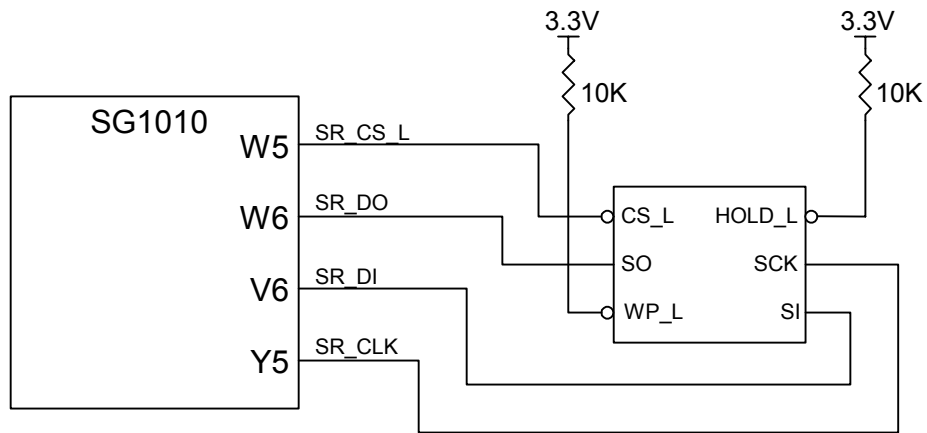
SG1010		SG2010	
Link A	Link B	Link A	Link B
0	1	0	1
1	2	0	1
2	3	0	1
3	4	0	1
4	5	0	1

Serial ROM Requirements

6.1 Serial ROM

Some applications will utilize the SG1010 serial ROM (SROM) interface to preload SG1010 registers at reset time. Since the interface is slow speed, typically 1Mhz, there are no special layout or implementation requirements. A high-frequency 0.1µF decoupling capacitor close to the power pin is recommended. An 8-pin, 3.3V device, such as an Atmel 25640A 8Kx8 serial EEPROM can be used for the serial ROM. An example SROM circuit can be seen in Figure 6–1. For more details on the SG1010 SROM interface refer to Section 3.10 of the SG1010 Hardware Reference Manual.

Figure 6–1 SROM Circuit



EMC Considerations

7.1 EMI Considerations

StarFabric links are based on Low Voltage Differential Signaling (LVDS) technology. Therefore, all emissions that are common mode or single ended are superfluous. Data collected on our reference board designs indicate the emissions at 622 Mhz (and its harmonics) are the main cause of concern.

There are generally two major ways to reduce emissions, shielding and filtering. We have reviewed our reference designs with industry leading EMC consultants and have developed the following recommendations:

- High quality shielded CAT5E cable assemblies reduce emissions substantially if used in conjunction with shielded modular connectors. The shielded modular connectors should be connected to chassis ground via a low inductance path.
- Use etch layout techniques such as plane splits to reduce the amount of radiation from the “noisy” planes to the “quiet” chassis ground. Crossing the splits with only the LVDS signals is ideal. Also, if there are any edges on the plane splits they should be chamfered (~45 degrees) to prevent antennas.
- Tightly matched etch lengths on differential pairs to reduce imbalance of the differential signal. Any imbalance becomes common mode noise and is most prevalent at multiples of 622Mhz.
- Chamfer the edges of the LVDS traces to remove any antennae effect
- Add high frequency capacitors (0.001uF) around the area where the LVDS traces are running. These capacitors are intended to suppress any high frequency noise that gets into the power/ground planes.
- Use gasketing around holes in the chassis to create a tighter RF seal.
- Use ferrite beads for LEDs placed on the chassis ground planes to filter out high frequencies from the “noisy” planes.
- Alternatively placing LEDs away from the chassis ground plane and using light pipes to conduct light to the edge panel.
- Use of common mode chokes on the transmit and receive LVDS pairs to filter out high frequency noise. (Impact on signal integrity should be assessed)

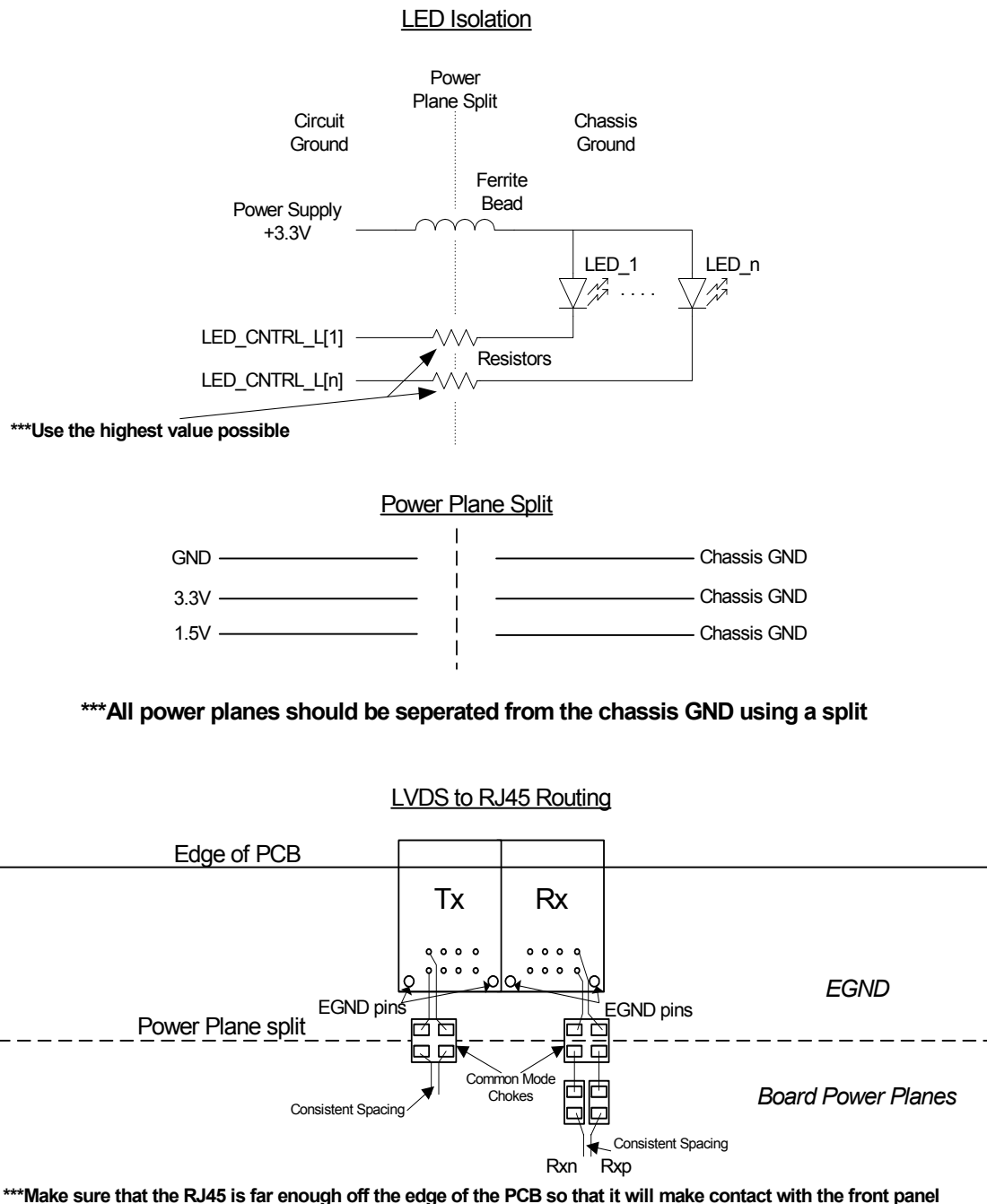
As a result of utilizing several of these EMI mitigation techniques StarGen's SFS2100 switch card and SGPCI64-A card met the following EMC emissions requirements:

EN 55022:1998 Class A ITE (EU)

FCC 47 CFR Part 15 Class A

Please see Figure for an example implementation.

Figure 7-1 EMI Design Considerations



7.2 ESD Considerations

All electronic devices are subject to damage from ElectroStatic Discharge (ESD). There are precautions that should be taken with all such devices throughout the stages of development including device (chip) handling, PCB handling and installation, and during normal functional operation. StarFabric devices have been designed to withstand ESD events on all device pins. StarGen devices fully meet the ESD Charged-Body Model and Human Body Model standards. In addition, StarGen boards and switches meet applicable system level standards. However, when designing boards and systems, designers should consider ESD as a possible threat especially if cable applications are being implemented.

There is a form of ESD associated with all links that use low loss cables such as Ethernet or CAT5E cables. The term Cable Discharge Event (CDE) is used to describe a statically charged cable being plugged into another device with resultant discharge and possible damage.

Shielded CAT5 or CAT5E cables, along with shielded connectors, are suggested as a good way to help prevent individual differential pair conductors from getting charged electrostatically.

Given the high speed low voltage nature of Starfabric links, it is important that any additional components that are used to protect the system from ESD be very low in capacitance so as not to adversely affect the link signal integrity during normal operation.

Stargen has experimented with devices such as Protek GBLC03 and found that they do provide additional protection and do not adversely affect link signal integrity.

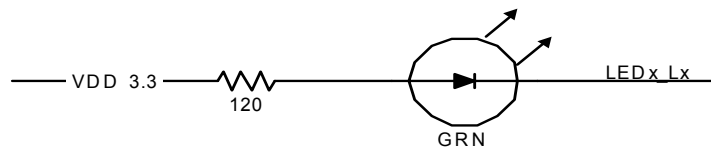
ESD protection devices for cable applications should be placed near the cable connector. If AC coupling capacitors and the common mode chokes are used the protection devices should be placed between them and the SG1010. The protection devices should have a solid low impedance connection to ground and they should be placed so that electrical stubs are minimized.

LED Usage

8.1 LED Overview

The SG1010 provides twenty-four signal pins, LED{5:0}_L[3:0], that can be used to drive external LEDs. The signals provide 24mA of drive current so that LEDs can be driven directly without the need for external components. The use of a current limiting resistor is recommended to ensure that the current flow is maintained below the 24mA limit.

Figure 8–1 Current limiting resistor



Two modes of operation are supported for the LED drive signals as follows:

1. Use of one LED for each differential pair status.
2. Use of one LED for each StarGen link (four differential pairs) status.

The mode is selected at reset by sampling the GPIO[0] (BGA location U9) signal. The single LED per link is recommended to reduce 3.3V power.

In addition to the use of LED signal pins for reporting link and differential pair status, direct control of LEDs with software is possible. Refer to the SG1010 Hardware Reference Manual for more information on software control of LEDs.

8.2 Use of One LED per LVDS Differential Pair

If the GPIO[0] signal is sampled low at reset, the LEDx_L[3:0] signals are enabled to drive a "0" for each differential pair that is in the synchronized state with traffic enabled (LED on). The LEDx_L[3:0] signals will drive a logic "1" for each differential pair that is not in the synchronized state with traffic enabled (LED off).

Use of One LED per StarGen Link

If a differential pair is synchronized but traffic is not enabled, then the associated LEDx_L[x] signal will toggle between a logic 1 and 0 with a period of ~500ms to blink the LED.

8.3 Use of One LED per StarGen Link

For some applications, the use of a single LED for a 4-differential pair link may be desired to reduce cost, power, and board real-estate. For these applications, the GPIO[0] signal should be pulled high at reset.

When GPIO[0] is sampled high at reset, the LEDx_L[0] signal is enabled to drive a "0" for each "link" that has at least one differential pair in the synchronized state with traffic enabled (LED on). The LEDx_L[0] signal will also drive a logic "1" to for each "link" that is not in the synchronized state with traffic enabled (LED off). The LED signal will be driven high only if all four differential pairs are either not synchronized or if their traffic enable bits are not set.

If a "link" is synchronized but traffic is not enabled, then the associated LEDx_L[0] signal will toggle between a logic 1 and 0 with a frequency of ~500ms to blink the LED.

Diagnostic Interfaces

9.1 JTAG

The SG1010 is fully compliant with the IEEE 1149.1a-1993 Boundary Scan Specification (known informally as "JTAG"). The SG1010 includes the following pins for IEEE 1149.1 support: TRST_L (Test Reset), TDI (Test Data In), TMS (Test Mode Select), TCK (Test Clock) and TDO (Test Data Out). The first four pins are input-only, while TDO is output-only.

For application that do not implement JTAG it is recommended that TRST_L is pulled down on the board. Designers should be aware that TRST_L has a 50K internal pull-up. All other input pins are also pulled high internally. TDO is an output-only and drives low when TRST is pulled high. The SG1010's implementation of IEEE 1149.1 includes the required instructions BYPASS, EXTEST, and SAMPLE/PRELOAD, and the optional instructions IDCODE and RUNBIST. The RUNBIST instruction is used to perform memory BIST (Built-in Self Test) only.

The SG1010 JTAG IDCODE is 32 bits long. The manufacturer IDCODE is 0000.0001.1101. The Part Number IDCODE is 0110.1111.1101.0000.

For more information, see the IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1-1990, IEEE Std. 1149.1a-1993, and IEEE Std. 1149.1b-1994.

For more information about SG1010 BSDL files contact StarGen customer support at support@stargen.com or visit the StarGen website, www.stargen.com.

9.2 Register Access Diagnostic Port

The SG1010 diagnostic port is used to read and write CSR's and other internal states during operation. The diagnostic port presents 16 registers to the user, each one byte wide. Four registers (A3- A0) are used to accumulate a 32-bit address, and four registers (D3- D0) are used to hold a Dword of data for the write or read. Registers A3- A0 reference a Channel 255 register offset within the SG1010. Two registers, TW and TR, are used to trigger the read or write to Channel 255 register space. Table 9-1 defines the registers and their addresses.

For more information regarding implementation of the diagnostic port please contact Stargen customer support at support@stargen.com.

Register Access Diagnostic Port

Table 9–1 Diagnostic Interface Register Addresses

Register Name	Address	Type
A0	0	R/W
A1	1	R/W
A2	2	R/W
A3	3	R/W
D0	4	R/W
D1	5	R/W
D2	6	R/W
D3	7	R/W
TW	8	R
TR	9	R
Reserved	A	—
Reserved	B	—
Reserved	C	—
Reserved	D	—
Reserved	E	—
Reserved	F	—

Glossary

BGA	Ball Grid Array
BRIDGE	An edge node that provides protocol translation; for example, a bridge between the fabric and a PCI bus.
CMOS	Complementary Metal-Oxide Semiconductor
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read-Only Memory
GPIO Signals	General Purpose I/O Signals
LED	Light-Emitting Diode
LVDS	Low Voltage Differential Signaling
PICMG	PCI Industrial Computer Management Group
PLL	Phase Lock Loop
PROM	Programmable Read-Only Memory
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
ROM	Read-Only Memory
SBC	Single Board Computers
SRAM	Serial Read-Only Memory
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
TTL	Transistor Transistor Logic