# SG2010 PCI to StarFabric Bridge in Industrial Temperature Applications

## Application Note

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STARGEN 1

# SG2010 at Industrial Temperature

## 1.1 Abstract

To ensure that the SG2010 PCI to StarFabric bridge operates properly in industrial temperature range applications, the use of an external 77.76 MHz clock source is required. The external clock source provides the SG2010 with appropriate clocking at temperatures ranging from -40ºC to +85ºC. The existing internal PLL supports a temperature range from 0ºC to 70ºC. This application note outlines the modifications required to implement the external clock source.

## 1.2 Clock Details

The SG2010 bridge has two distinct types of PLLs, one associated with the clock-data recovery (CDR) in the SERDES, and a global PLL that generates a clock for internal logic. Both the CDR and global PLLs use the 62.208 MHz reference input clock.

The global PLL implements a multiply/divide clock multiplication function. The resulting internal global clock is roughly 78 MHz in the SG2010. This PLL goes through an auto-trimming process to optimize it's performance. The synthesized 78 MHz clock is appropriate for all applications rated for a temperature range from 0ºC to 70ºC.

However when using the SG2010 in an environment outside of the commercial 0ºC to +70ºC specification, the global PLL is not guaranteed to function properly. An external clock source is required for these applications. Note that the 62.208 MHz reference clock is still required for the CDR when the global PLL is being bypassed.

## 1.3 Design Guidelines

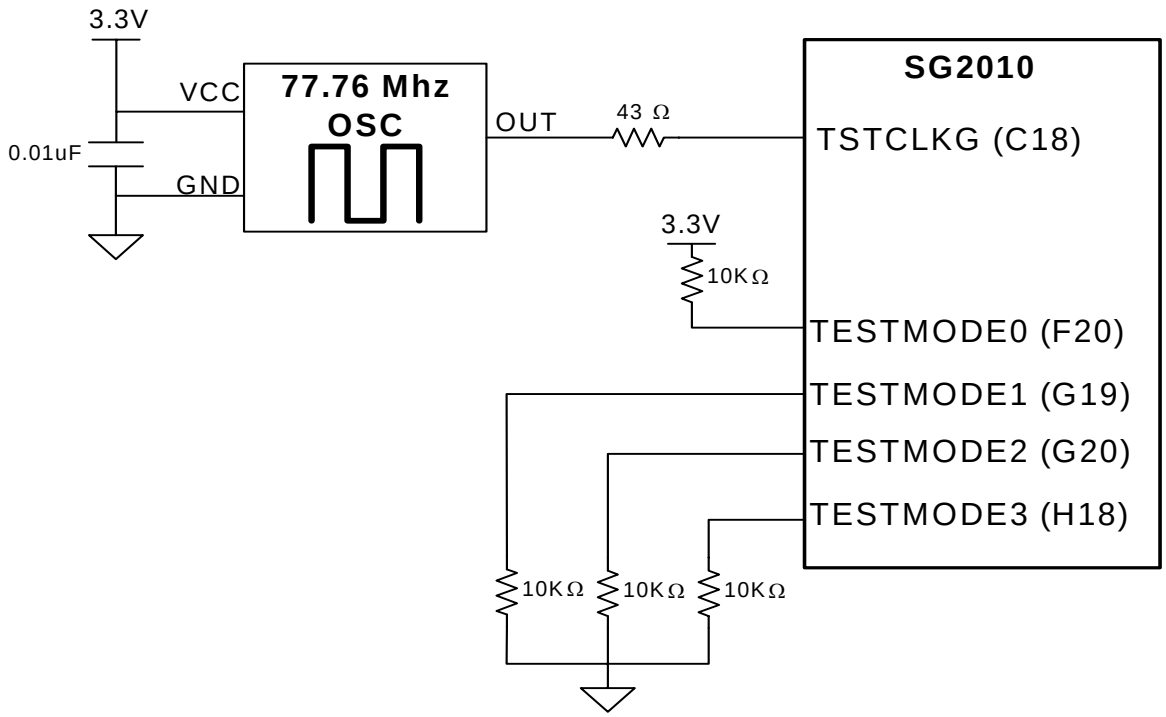
When using the SG2010 above the 70 degree C commercial specification, the internal global PLL needs to be bypassed and an external 77.76 MHz clock source is to be used. The hardware implementation is shown in Figure 1–1 and described below:

1. Set the SG2010 into PLL bypass mode by setting the TESTMODE<3:0> inputs to a <0001>, thereby forcing the SG2010 to use an external 77.76 MHz oscillator instead of the internally generated clock. The TESTMODE<3:0> signals are located at BGA ball positions H18, G20, G19, and F20 respectively. TEST-

MODE<3:1> can be signaled low with pull-down resistors and TESTMODE<0> can be signaled high with a pull-up resistor.

2. Connect a 77.76 MHz clock oscillator to the TSTCLKG signal pin (BGA ball C18) of the device. Include an appropriate value series damping resistor between the clock oscillator's output and the SG2010's TSTCLKG input. This resistor should be placed close to the source of the clock.

**Figure 1–1 Recommended Modification**




## Oscillator Specifications

Frequency: 77.76 MHz 100ppm

Jitter: 150ps peak-to-peak max

Duty Cycle: 45/55% min/max

Voltage Supply: 3.3 Volts DC

Operating Temperature:-40°C to 85°C

# 2 References/ Contacts

## 2.1 References

- SG2010 PCI to StarFabric Bridge Hardware Reference Manual
- SG2010 PCI to StarFabric Bridge Data Sheet
- SG2010 PCI to StarFabric Bridge Hardware Implementation Guide

## 2.2 Contact Information

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